Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	186693	(controller control bridge regulator) near6 (ram memory cache)	USPAT	OR	ON	2005/03/29 11:48
S2	3485	S1 with refresh	USPAT	OR	ON	2005/03/29 10:59
S3	64	S2 same (backup auxiliary secondary)	USPAT	OR	ON	2005/03/29 11:01
S4	72394	power adj2 (controller control bridge regulator)	USPAT	OR	ON	2005/03/29 12:20
S5	111	S4 near8 (memory adj (control controller regulator))	USPAT	OR	ON	2005/03/29 11:47
S6	4	S5 with (during while)	USPAT	OR	ON	2005/03/29 11:13
S7	49244	(ram memory cache) adj (management controller control bridge regulator)	USPAT	OR	ON	2005/03/29 11:51
S8	227	(while during after) near3 (self$1refresh)	USPAT	OR	ON	2005/03/29 11:49
S9	301	(while during after) near6 (self$1refresh)	USPAT	OR	ON	2005/03/29 11:49
S10	12	S9 with S7	USPAT	OR	ON	2005/03/29 11:49
S11	1131	S7 near8 (off shut$3 stop$3)	USPAT	OR	ON	2005/03/29 11:52
S12	88	S11 with power	USPAT	OR	ON	2005/03/29 11:53
S13	204	S4 same refresh	USPAT	OR	ON	2005/03/29 12:21